ॐ

SASURIE COLLEGE OF ENGINEERING

Approved by AICTE, New Delhi. Affiliated to Anna University, Chennai

Near NH544, Coimbatore Bypass, Near Vijayamangalam Tollgate,Tirupur 638056

NAAC DOCUMENTS

QUALITY INDICATOR FRAME WORK

CRITERION - 1

CURRICULAR ASPECTS

SUBMITTED BY

IQAC

INTERNAL QUALITY ASSURANCE CELL

SASURIE COLLEGE OF ENGINEERING

Criterion 1	Curricular Aspects	100

1.1 Curricular Planning and Implementation (20)

1.1.1The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment

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SASURIE
College of Engineering
Vijayamangalam, Tirupur

Department : Electronics & Communication Engineering
Subject Code & Name : EC6703/Embedded & Real Time systems
Class & Batch : IV ECE / 2015-2019
Semester : VII

CONTENTS – COURSE FILE

S.NO	PARTICULARS	REMARKS
1	Time Table	Hardcopy
2	Student name list	Hardcopy
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4	Subject Information Record	Hard copy
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6	Lesson Plan	Hardcopy
7	Test Plan for the Subject	Hard copy
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9	Corrective Action Report	Hard copy(new format)
10	Quality objective monitoring record	Hard copy
11	Internal test mark sheet(Consolidated)	Hard copy
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15	Sample Answer paper for all test(Min-3)	Hard copy
16	Content beyond the syllabus	Soft copy
17	Tutorial Class – schedule and content	Hard copy
18	Assignment – schedule and paper	Hard copy
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21	Question bank	Soft copy
22	Sample university question papers(min 5 QP-recent exam)	Soft copy
23	Lecture Note	Hard copy
24	Special Class if any, Approval letter, Schedule, content covered.	Hard copy
25	Spark faculty score, student score	Hard copy

	Prepared By	Approved By
Sign:		
Name:	Mr.G.Johny	Mr.S Gladson
	Faculty	HD

Dr.M.VIJAYAKUMAR ME., Ph.D.,
PRINCIPAL
SASURIE COLLEGE OF ENGINEERING,
Vijayamangalam - 638 056, Tirupur (Dt).

SASURIE
College of Engineering
Vijayamangalam, Tiruppur.

Name :
Designation :

CLASS TIME TABLE- Academic Year 2018-19- Odd Semester

Year: IV / SEM: VII

HOUR	8.58a.m. TO 9.00a.m	I	II	10.40a.m. TO 10.55a.m.	III	IV	12.35 p.m. TO 1.20 p.m.	V	VI	2.50p.m. 3.00p.m.	VII	VIII
DAY/ TIME		9.00 a.m. TO 9.50 a.m.	9.50 a.m. TO 10.40 a.m.		10.55 a.m. TO 11.45 a.m.	11.45 a.m. TO 12.35 p.m.		1.20 p.m. TO 2.05 p.m.	2.05p.m. TO 2.50p.m.		3.00 p.m TO 3.45p.m	3.45 p.m. TO 4.30 p.m.
MON	PRAYER			BREAK			LUNCH			BREAK		ERTS
TUE												
WED					ERTS				ERTS			
THU		ERTS /ACT										
FRI						ERTS						
SAT												

S.No	Subject Code		Name of the Subject	Branch & Semester	No of hours
1	EC6504	ERTS	Embedded & Real Time systems	ECE & VII	5
			TOTAL		5

	Prepared by	Verified by	Authorised by
Sign:			
Name:	Mr.G.Johny	Mr.S.Madhan	
	Time Table Incharge	HOD/ECE	

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ECE Final year NAME LIST

S.No	Register Number	Name of the student
1	732415106002	ANTHONYRAJ D
2	732415106003	ARCHANA S
3	732415106004	BHARATHKUMAR M
4	732415106005	DEEPIKARANI M
5	732415106006	DHANABALAN P
6	732415106007	DHIVYADHARSHINI S
7	732415106008	DIVYABHARATHI M
8	732415106009	ELAVARASI S
9	732415106010	GOWTHAM A
10	732415106011	GRACE THEBORAL P
11	732415106012	JANAKI N
12	732415106013	JEEVANANTHAM L
13	732415106014	KALIYAMMAL S
14	732415106015	KAMALASHRI S
15	732415106016	KARTHIK R
16	732415106017	KEERTHANA L
17	732415106018	KOWSHIKA R
18	732415106019	LAVANYA R
19	732415106020	LOGANAYAHI D
20	732415106021	MANOJ S
21	732415106022	MERLIN PREETHI A
22	732415106023	MONISHA S
23	732415106024	MOUNIKA K
24	732415106025	NANDHINI S
25	732415106026	NANDHINI V
26	732415106027	NAVEENKUMAR S
27	732415106028	PADMAPRIYA M
28	732415106029	PADMAPRIYA V
29	732415106031	PAVITHRA T
30	732415106032	POONKODI P
31	732415106034	RAJESWARI S
32	732415106035	RAMUTHAI S
33	732415106036	RANJITHA V
34	732415106037	REETHIGA S
35	732415106038	REVATHI K
36	732415106039	RUBA N
37	732415106040	SANJEV V
38	732415106041	SATHISHKUMAR D
39	732415106042	SELVAKUMAR K
40	732415106043	SHANMATHI G
41	732415106044	SIVARANJINI R
42	732415106045	SUMITHRA D
43	732415106046	SUVETHA U
44	732415106047	TAMILARASU N
45	732415106048	VEERESWARI T
46	732415106049	VIJAYALAKSHMI M
47	732415106050	YASODHA S

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SASURIE College of Engineering

Department of ECE
Student Arrear List

Class: IV ECE
Semester: VII
Academic Year: 2018-2019

S.NO	ROLL NO	NAME	No of Arrears
1	732415106002	ANTHONYRAJ.D	4
2	732415106003	ARCHANA.S	5
3	732415106004	BHARATHKUMAR.M	8
4	732415106005	DEEPIKARANI.M	10
5	732415106006	DHANABALAN.P	20
6	732415106007	DHIVYADHARSHINI.S	4
7	732415106008	DIVYABHARATHI.M	6
8	732415106009	ELAVARASI.S	3
9	732415106010	GOWTHAM.A	1
10	732415106011	GRACE THEBORAL.P	3
11	732415106012	JANAKI.N	0
12	732415106013	JEEVANANTHAM.L	9
13	732415106014	KALIYAMMAL.S	0
14	732415106015	KAMALASHRI.S	1
15	732415106016	KARTHIK.R	2
16	732415106017	KEERTHANA.L	13
17	732415106018	KOWSHIKA.R	0
18	732415106019	LAVANYA.R	1
19	732415106020	LOGANAYAHI.D	1
20	732415106021	MANOJ.S	3
21	732415106022	MERLIN PREETHI.A	4
22	732415106023	MONISHA.S	1
23	732415106024	MOUNIKA.K	7
24	732415106025	NANDHINI.S	1
25	732415106026	NANDHINI.V	4
26	732415106027	NAVEENKUMAR.S	14
27	732415106028	PADMAPRIYA.M	2
28	732415106029	PADMAPRIYA.V	6
29	732415106031	PAVITHRA.T	2
30	732415106032	POONKODI.P	2
31	732415106034	RAJESWARI.S	1
32	732415106035	RAMUTHAI.S	3
33	732415106036	RANJITHA.V	0
34	732415106037	REETHIGA.S	12
35	732415106038	REVATHI.K	1
36	732415106039	RUBA.N	6
37	732415106040	SANJEV.V	0
38	732415106041	SATHISHKUMAR.D	18
39	732415106042	SELVAKUMAR.K	20
40	732415106043	SHANMATHI.G	3
41	732415106044	SIVARANJINI.R	2
42	732415106045	SUMITHRA.D	1
43	732415106046	SUVETHA.U	0
44	732415106047	TAMILARASU.N	11
45	732415106048	VEERESWARI.T	2
46	732415106049	VIJAYALAKSHMI.M	7
47	732415106050	YASODHA.S	1

	Prepared by	Verified by
SIGN		
NAME	Mr.G.Johny	Mr.S.Gladson
	CLASS ADVISOR	HD

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EC6703 EMBEDDED AND REAL TIME SYSTEMS

L T P C
3 0 0 3

OBJECTIVES:

The student should be made to:

- Learn the architecture and programming of ARM processor.
- Be familiar with the embedded computing platform design and analysis
- Be exposed to the basic concepts of real time Operating system
- Learn the system design techniques and networks for embedded systems

UNIT I INTRODUCTION TO EMBEDDED COMPUTING AND ARM PROCESSORS 9

Complex systems and micro processors– Embedded system design process –Design example: Model train controller- Instruction sets preliminaries - ARM Processor – CPU: programming input and output- supervisor mode, exceptions and traps – Co-processors- Memory system mechanisms – CPU performance- CPU power consumption.

UNIT II EMBEDDED COMPUTING PLATFORM DESIGN 9

The CPU Bus-Memory devices and systems–Designing with computing platforms – consumer electronics architecture – platform-level performance analysis - Components for embedded programs- Models of programs- Assembly, linking and loading – compilation techniques- Program level performance analysis – Software performance optimization – Program level energy and power analysis and optimization – Analysis and optimization of program size- Program validation and testing

UNIT III PROCESSES AND OPERATING SYSTEMS 9

Introduction – Multiple tasks and multiple processes – Multirate systems- Preemptive real-time operating systems- Priority based scheduling- Interprocess communication mechanisms – Evaluating operating system performance- power optimization strategies for processes – Example Real time operating systems-POSIX-Windows CE.

UNIT V SYSTEM DESIGN TECHNIQUES AND NETWORKS 9

Design methodologies- Design flows - Requirement Analysis – Specifications-System analysis and architecture design – Quality Assurance techniques- Distributed embedded systems – MPSoCs and shared memory multiprocessors.

UNIT V CASE STUDY 9

Data compressor - Alarm Clock - Audio player - Software modem-Digital still camera - Telephone answering machine-Engine control unit – Video accelerator.

TOTAL: 45 PERIODS OUTCOMES:

Upon completion of the course, students will be able to:

- Describe the architecture and programming of ARM processor.
- Outline the concepts of embedded systems
- Explain the basic concepts of real time Operating system design
- Use the system design techniques to develop software for embedded systems
- Differentiate between the general purpose operating system and the real time operating system
- Model real-time applications using embedded-system concepts

TEXT BOOK:

1. Marilyn Wolf, "Computers as Components - Principles of Embedded Computing System Design" Third Edition "Morgan Kaufmann Publisher (An imprint from Elsevier), 2012

REFERENCES:

1. Jonathan W Valvano, "Embedded Microcomputer Systems Real Time Interfacing", Third Edition Cengage Learning, 2012
2. David E. Simon, "An Embedded Software Primer", 1st Edition, Fifth Impression, Addison-Wesley Professional, 2007.
3. Raymond J.A. Buhr, Donald L Bailey, "An Introduction to Real-Time Systems- From Design to Networking with C/C++", Prentice Hall, 1999
4. C M Krishna, Kang G. Shin, "Real-Time Systems", International Editions, Mc Graw Hill 1997
5. K.V.K.K Prasad, "Embedded Real-Time Systems: Concepts, Design & Programming", Dream Tech Press 2005
6. Sriram V Iyer, Pankaj Gupta, "Embedded Real Time Systems Programming", Tata Mc Graw Hill, 2004

	Prepared By	Approved By
Sign:		
Name:	Mr.G.Johny	Mr.S.Gladson
	Faculty	HD

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(Accredited by NAAC, Under 2f and 12B status)

LESSON PLAN

ulty Name : G.JOHNY
Designation: Assistant Professor

partment : ECE
Semester/ Year: VII / IV

bject / Code : EMBEDDED & REAL TIME SYSTEM/EC 6703

ademic Year : 2018-2019

No.	Proposed Date	Proposed Period	Details of Topic Covered	TA	Ref.	Actual Date	Actual Period	Remarks
UNIT-I-INTRODUCTION TO EMBEDDED COMPUTING & PROCESSORS								
1	2/7/2018	8	Introduction to course and outcomes	3	1	02/07/18	8	
2	4/7/2018	3	Complex system and micro processors	3	1	04/07/18	3	
3	4/7/2018	6	Embedded system design process	3	1	04/07/18	6	
4	5/7/2018	1	Model train controller	3	1	05/07/18	1	
5	6/7/2018	4	Instruction set preliminaries	3	1	06/07/18	4	
6	9/7/2018	8	Instruction set preliminaries	3	1	07/07/18	5	
7	11/7/2018	3	ARM processor – CPU: Programming Input and output	3	1	07/07/18	6	
8	11/7/2018	6	Supervisor mode, exceptions and traps	3	1	09/07/18	8	
9	12/7/2018	1	Slip test			12/07/18	1	
10	13/7/2018	4	Co-processors-Memory system mechanisms	3	1	13/07/18	4	
11	16/7/2018	8	CPU Performance and consumption	3	1	14/07/18	3	
UNIT-II-EMBEDDED COMPUTING & PLATFORM DESIGN								
12	18/7/2018	3	CPU Bus-Memory devices and systems	3	1	14/07/18	7	
13	18/7/2018	6	Designing with computing platforms	3	1	16/07/18	2	
14	19/7/2018	1	~~Slip test~~ PLATFORM ANALYSIS.	3	1	16/07/18	8	
15	25/7/2018	6	Consumer Electronics architecture	3	1	18/07/18	8	
16	1/8/2018	3	Platform level performance analysis	3	1	19/07/18	6	
17	1/8/2018	6	Components for embedded programs and modes of programs	3	1	24/07/18	6	
18	2/8/18	1	Slip test			22/08/18	1	
19	3/8/18	4	Assembly, linking and loading	3	1	04/08/18	3	
20	6/8/18	8	Program level energy and power analysis	3	1	04/08/18	4	
21	8/8/18	3	Software performance optimization	3	1	04/08/18	6	
22	8/8/18	6	Program validation and testing	3	1	06/08/18	8	
UNIT III- PROCESSES & OPERATING SYSTEMS								

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						7/8/18	1	
23	9/8/2018	1	Slip test	3	1	14/8/18	6	
24	10/8/2018	4	Multiple tasks and multiple process	3	1	15/8/18	8	
25	13/8/2018	8	Multirate systems and preemptive RTOS	3	1	16/8/18	1	
26	16/8/2018	1	~~Slip test~~ RTOS	3	1	23/8/18	1	
27	20/8/2018	8	Inter process communication mechanisms	3	1	24/8/18	4	
28	23/8/2018	1	~~Slip test~~ SCHEDULING.	3	1	27/8/18	8	
29	29/8/2018	6	Application based process	3	1	29/8/18	4	
30	31/8/2018	4	Power optimization strategies for processes	3	1	30/8/18	7	
31	3/9/2018	8	Real time operating system	3	1	30/8/18	2	
32	5/9/2018	3	POSIX-Windows CE					
			UNIT IV-SYSTEM DESIGN TECHNIQUES & NETWORKS					
33	5/9/2018	6	Design methodologies	3	1	31/8/18	4	
34	6/9/2018	1	~~Slip test~~ NETWORK MANAGEMENT	3	1	17/9/18	7	
35	7/9/2018	4	Design flows of networks	3	1	17/9/18	2	
36	10/9/2018	8	Requirement analysis	3	1	17/9/18	8	
37	12/9/2018	3	Specifications of RTOS	3	1	18/9/18	2	
38	12/9/2018	6	System analysis and architecture design	3	1	18/9/18	5	
39	17/9/2018	8	Quality assurance techniques	3	1	20/9/18	1	
40	19/9/2018	3	Distributed embedded systems	3	1	22/9/18	3	
41	19/9/2018	6	MPSoC's and Architecture	3	1	22/9/18	6	
42	20/9/2018	1	~~Slip test~~ ARM PROCESSOR	3	1	24/9/18	8	
			UNIT V-CASE STUDY					
43	24/9/2018	8	Case study on Data compressor	3	1	26/9/18	5,6	
44	26/9/2018	3	Case study on Alarm clock	3	1	27/9/18	1,5	
45	26/9/2018	6	Case study on Audio player	3	1	28/9/18	8	
46	27/9/2018	1	Case study on Software modem	3	1	29/9/18	3	
47	28/9/2018	4	Case study on Digital still camera	3	1	29/9/18	6	
48	1/10/18	8	Case study on Telephone answering machine	3	1	1/10/18	8	
49	3/10/18	3	Case study on Engine control unit	3	1	3/10/18	1	
50	3/10/18	6	Case study on Video accelerator	3	1	4/10/18	1	

Reference books (Ref):

1 K. V K K Prasad "Embedded & Real time systems concept, Design & programming" Dream tech process 2005

2 Marilyn wolf." Computers as components" Third Edition 2012

Teaching Aids (TA):

1 Black Board with Chalk

2 Overhead Projector

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3. LCD Projector

4. Others (Field visits, Charts, Comet Models)

	Prepared by		
Sign			
Name	G. Sabari		
	Faculty	HOD	Principal

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SASURIE
College of Engineering
Vijayamangalam, Tirupur

Department of Electronics and Communication Engineering

SUBJECT INFORMATION RECORD

Department	: ECE
Subject	: EC6703 / Embedded & Real Time systems
Year	: IV
Semester	: VII
Last year handled by	: Mr. Syed kasim
Percentage of Result (last year)	: 64%
Quality Objectives	: To obtain 80 Percentage of result in Unit Tests and Anna university examinations.

REFERENCES:

1. Jonathan W.Valvano, "Embedded Microcomputer Systems Real Time Interfacing", Third Edition Cengage Learning, 2012.
2. David. E. Simon, "An Embedded Software Primer", 1st Edition, Fifth Impression, Addison-Wesley Professional, 2007.
3. Raymond J.A. Buhr, Donald L.Bailey, "An Introduction to Real-Time Systems- From Design to Networking with C/C++", Prentice Hall, 1999.
4. C.M. Krishna, Kang G. Shin, "Real-Time Systems", International Editions, Mc Graw Hill 1997
5. K.V.K.K.Prasad, "Embedded Real-Time Systems: Concepts, Design & Programming", Dream Tech Press, 2005.
6. Sriram V Iyer, Pankaj Gupta, "Embedded Real Time Systems Programming", Tata Mc Graw Hill, 2004.

	Prepared By	Approved By
Sign:		
Name:	Mr.G.Johny	Mr.S Gladson
	Faculty	HD

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SASURIE College of Engineering
Vijayamangalam, Tirupur

Department of Electronics and Communication Engineering

TEST PLAN FOR SUBJECT

Subject : EC6703 / Embedded & Real Time systems Faculty: Mr.G.Johny,AP/ECE

Semester : VII Year: IV

Department : ECE

S. No.	Description	Planned Date/Month	Actual Conducted Date / Month	Remarks
1	Internal Test-I	23.07.18 to 28.07.18	25.07.18	
2	Internal Test II	01.09.18 to 07.09.18	04.09.18	
3	Model Examination	08.10.18 to 13.10.18	11.10.18	

	Prepared By	Approved By
Sign:		
Name:	Mr.G.Johny	Mr.S.Gladson
	Faculty	HD

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SASURIE College of Engineering
Vijayamangalam, Tirupur

DEPARTEMNT OF ELECTRONICS & COMMUNICATION ENGINEERING

CLASS : IV

Date: 30.10.2018

Subject Code/Name : EC 6703 / EMBEDDED & REAL TIME SYSTEMS

Subject Handling Faculty Name : Ms.R.Jesintha

S.No	Registration Number	Student Name	Slip test 1	Internal test 1	Slip test 2	Slip test 3	Internal test 2	MODEL	MODEL AFTER RE TEST
1	732415106002	ANTHONYRAJ.D	88	83	88	76	70	43	43
2	732415106003	ARCHANA.S	AAA	AAA	AAA	AAA	AAA	AAA	71
3	732415106004	BHARATHKUMAR.M	88	89	84	76	88	AAA	87
4	732415106005	DEEPIKARANI.M	96	82	84	84	88	84	84
5	732415106006	DHANABALAN.P	88	64	84	68	60	49	49
6	732415106007	DHIVYADHARSHINI.S	80	88	68	AAA	76	77	77
7	732415106008	DIVYABHARATHI.M	92	88	88	76	92	80	80
8	732415106009	ELAVARASI.S	96	77	72	64	85	78	78
9	732415106010	GOWTHAM.A	76	71	52	68	69	70	70
10	732415106011	GRACE THEBORAL.P	AAA	81	52	68	70	74	74
11	732415106012	JANAKI.N	92	96	88	88	89	85	85
12	732415106013	JEEVANANTHAM.L	72	75	76	36	64	48	48
13	732415106014	KALIYAMMAL.S	96	88	AAA	68	84	84	84
14	732415106015	KAMALASHRI.S	96	93	92	80	68	91	91
15	732415106016	KARTHIK.R	64	78	48	68	64	68	68
16	732415106017	KEERTHANA.L	92	81	AAA	AAA	71	57	57
17	732415106018	KOWSHIKA.R	80	87	80	72	75	75	75
18	732415106019	LAVANYA.R	AAA	77	84	88	70	73	73
19	732415106020	LOGANAYAHI.D	96	85	AAA	60	70	AAA	85
20	732415106021	MANOJ.S	44	62	56	68	59	65	65
21	732415106022	MERLIN PREETHI.A	96	86	AAA	68	86	84	84
22	732415106023	MONISHA.S	96	84	AAA	AAA	82	83	83
23	732415106024	MOUNIKA.K	84	68	AAA	52	83	63	63
24	732415106025	NANDHINI.S	96	79	84	56	64	82	82

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	732415106026	NANDHINI.V	AAA	61	76	84	91	84	84
	732415106027	NAVEENKUMAR.S	76	64	60	64	66	52	52
	732415106028	PADMAPRIYA.M	96	73	80	80	78	73	73
	732415106029	PADMAPRIYA.V	92	83	68	76	91	91	91
	732415106031	PAVITHRA.T	92	81	84	88	83	75	75
	732415106032	POONKODI.P	96	85	92	84	92	87	87
	732415106034	RAJESWARI.S	64	60	AAA	AAA	AAA	71	71
	732415106035	RAMUTHAI.S	88	75	80	80	78	78	78
	732415106036	RANJITHA.V	92	85	64	76	83	87	87
	732415106037	REETHIGA.S	96	82	AAA	AAA	77	56	56
	732415106038	REVATHI.K	96	74	AAA	88	88	82	82
	732415106039	RUBA.N	96	79	AAA	AAA	86	70	70
	732415106040	SANJEV.V	88	83	92	64	69	80	80
	732415106041	SATHISHKUMAR.D	64	69	68	44	AAA	AAA	44
	732415106042	SELVAKUMAR.K	40	45	32	40	23	27	27
	732415106043	SHANMATHI.G	92	77	80	72	82	71	71
	732415106044	SIVARANJINI.R	92	76	AAA	68	91	67	67
	732415106045	SUMITHRA.D	96	72	80	84	80	74	74
	732415106046	SUVETHA.U	96	85	80	84	88	82	82
	732415106047	TAMILARASU.N	64	67	AAA	56	52	66	66
	732415106048	VEERESWARI.T	96	60	72	76	64	69	69
	732415106049	VIJAYALAKSHMI.M	88	85	84	68	84	79	79
	732415106050	YASODHA.S	80	74	64	44	71	74	74

otal number of students :		47	47	47	47	47	47	47
o. of students attended :		43	46	34	40	44	43	43
lo. of students Absent :		4	1	13	7	3	4	4
lo. of students pass:		43	45	30	33	41	43	43
lo. of students failed:		1	1	4	7	3	1	1
Pass Percentage :		97.67	97.82	88.23	82.5	93.18	97.7	97.7

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Department of Electronics and Communication Engineering

RESULT ANALYSIS OF TEST & CORRECTIVE ACTION PLAN

Subject code & Name: EC6703 & Embedded & Real Time systems Date: 27.07.2018

Class: IV ECE Semester VII

Exam details & date	: INTERNAL TEST I & 25.07.2018
Faculty	:
Number of students	: 47
No. of students attended	: 40
No. of students absent	: 7
No. of students passed	: 39
No. of students failed	: 01
Overall Percentage	: 97.5%

RESULT DATA:

Marks	0-25	26-50	51-75	76-90	91-100
No. of Students	-	1	16	27	2

	Prepared By	Approved By
Sign:		
Name:	JOHNY.G	GLADSON S
	Faculty	HD

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Department of Electronics and Communication Engineering

RESULT ANALYSIS OF TEST & CORRECTIVE ACTION PLAN

Subject : EC6703 –Embedded & Real Time systems

Date: 07.09.2018

Class : IV ECE

Department: ECE

Semester : VII

Exam details & date : INTERNAL TEST II & 04.09.2018

Faculty :

Number of students : 47

No. of students attended : 44

No. of students absent : 03

No. of students passed : 41

No. of students failed : 03

Overall Percentage : 93.18

RESULT DATA:

Marks	0-25	26-50	51-75	76-90	91-100
No. of Students	1	-	16	22	5

	Prepared By	Approved By
Sign:		
Name:	JOHNY.G	GLADSONS
	Faculty	HD

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Department of Electronics and Communication Engineering

RESULT ANALYSIS OF TEST & CORRECTIVE ACTION PLAN

Subject : EC6703 –Embedded & Real Time systems Date: 14.10.2018

Class : IV ECE

Semester : VII Department: ECE

Exam details & date : MODEL EXAMINATION & 11.10.2018

Faculty :

Number of students : 47

No. of students attended : 47

No. of students absent : NIL

No. of students passed : 40

No. of students failed : 07

Overall Percentage : 85.1

RESULT DATA:

Marks	0-25	26-50	51-75	76-90	91-100
No. of Students	-	5	19	21	2

	Prepared By	Approved By
Sign:	R. Johny	
Name:	JOHNY. G.	GLADSONS
	Faculty	HD

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Vijayamangalam, Tirupur

Department of Electronics and Communication Engineering

RESULT ANALYSIS OF TEST & CORRECTIVE ACTION PLAN

Subject : EC6703 –Embedded & Real Time systems Date: 14.10.2018

Class : IV ECE

Semester : VII Department: ECE

Exam details & date : MODEL EXAMINATION & 11.10.2018

Faculty :

Number of students : 47

No. of students attended : 47

No. of students absent : NIL

No. of students passed : 40

No. of students failed : 07

Overall Percentage : 85.1

RESULT DATA:

Marks	0-25	26-50	51-75	76-90	91-100
No. of Students	-	5	19	21	2

	Prepared By	Approved By
Sign:	R. Johny	
Name:	JOHNY. G1.	GLADSONS
	Faculty	HD

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CORRECTIVE ACTION REPORT

DEPT : ECE **YEAR : IV**

SUBJECT: EC6703/EMBEDDED & REAL TIME SYSTEMS **SEMESTER : VII**

S.No	Internal Test	Percentage of marks	Root Cause (Metrics)	Corrective Action	Deadline date	Remarks
1	I	97%	6 students got absent due to their friends mother passed away Lagging of presentation of a student leads to failure	Conducted retest for those 6 students by providing various question paper	-	-
2	II	93.18 /	Due to the questions are asked in Design Power, they spend minimum Examples	Technical Papers Designed as per the Video presentation.	-	-
3	III (Model Examination)	85.11.	Due to Time management & Lagging of Presentation Skills.	Conducted Weekly class and explained about time Constraint to finish the Courses on time.	-	-

	Prepared By	Approved By
Sign:	R. Johny	
Name:	JOHNY.G1	GLADSON T.S
	Faculty	HD

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QUALITY OBJECTIVE MONITORING RECORD

Department : ECE

Year : IV ECE

Semester : VII

Subject : EC6703 & Embedded Real Time systems

S.No	Quality Objective	InternalTest-I		InternalTest-II		Model Examination	
		Expecting result	Obtained result	Expecting result	Obtained result	Expecting result	Obtained result
1	>=80%	>=90%	97%	≥ 85%	93.18%	≥ 85%	85.1%

	Prepared By	Approved By
Sign:	R. Jeni	SG
Name:	JOHNY. G	Mr S Gladson
	Faculty	HOD

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Register Number:												

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Model exam			Date/Session	11.10.2018	Marks	100
Course code	EC6703	Course Title	Embedded and Real Time Systems			
Regulation	2017	Duration	3 Hours	Academic Year	2018-2019	
Year	VI	Semester	VII	Department	ECE	

COURSE OUTCOMES

CO1:	Learn the architecture and programming of ARM processor.
CO2:	Be familiar with the embedded computing platform design and analysis
CO3:	Be exposed to the basic concepts of real time operating systems.
CO4:	Learn the system design techniques and networks for embedded systems

Q.No.	Question	CO	BTS
	PART A (Answer all the Questions 10 x 2 = 20 Marks)		
1	What is the average memory access time of a machine whose bit rate is 93% with a cache access time of 5 ns and a main memory access time of 80 ns?	CO1	R
2	Distinguish between requirement and specification.	CO1	AN
3	What is a bridge? Where it is applied?	CO2	R
4	Draw the data flow graph for the block shown below?	CO2	C
5	What is a semaphore?	CO3	R
6	Which should have lower overhead a pre-emptive or co-operative context switch mechanism?	CO3	R
7	State the need for accelerators.	CO3	R
8	Difference between fixed priority arbitrations and round robin arbitration.	CO4	AN
9	What do you mean by co-design?	CO4	R
10	List out the advantages of set-top-box.	CO4	AN
	PART B (Answer all the Questions 5 x 13 = 65 Marks)		
11a	Develop the requirement, specification and state diagram of a model train controller.	CO1	AP
	OR		
11b	Draw the architecture of an ARM processor. Explain about the various blocks in detail.	CO1	C
12a	With a suitable example explain how logic analyzer in circuit emulator and Co-simulator are used in debugging tools.	CO2	U
	OR		
12b	Discuss about design pattern, loop transformation and scheduling.	CO2	C
13a	i)Explain why an automobile engine required multirate control. (6)	CO3	U

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	iii) Explain the earliest deadline-first scheduling, compare performance with the Scheduling algorithms. (7)	CO3	U
	OR		
13b	Describe in detail about the scheduling policies with suitable examples	CO3	R
14a	Explain about accelerated system design with suitable diagrams	CO3	U
	OR		
14b	Discuss in detail about the distributed embedded architecture.	CO3	C
15a	Describe in detail about the principle of operation of software modem.	CO2	R
	OR		
15b	What are FOSS tools for embedded system development? Explain the tools in detail	CO3	R
	PART C (Answer all the Questions 1x15 = 15 Marks)		
16a	Write a program on LED segmented by 8 bits with a flow chart.	CO3	C
	OR		
16b	Write a program on LCD & its switching characteristics with a suitable flow chart	CO3	C

10/10/18
Course Faculty
(Name /Sign / Date)
G. JOHNY

10/10/18
HOD
(Name /Sign / Date)
S. Gladson

Principal
(Name /Sign / Date)
Dr. K. Pandiaraj
DR. M. VIJAYAKUMAR M.E., Ph.D.
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Internal Assessment Test Answer Book

Name	V. Padmapriya			Year/ Semester/Section	IV EVII
Register Number	732415106029	Date/Session	11.10.2018FN	Department	ECE
Course code	EC67032	Course Title	Embedded & Real time Systems		
Internal Assessment Test	IAT 1 ☐	IAT 2 ☐	IAT 3 ☐	Model	☑
Name and Signature of the Invigilator with date					

Instruction to the Student: Put tick mark to the question attended in the column against question.

Part A			Part B/ Part C						Total Marks
Q. No.	✓	Marks	Q. NO.	✓	a Marks	✓	b Marks		
1	✓	2	11	✓	12				12
2	✓	2	12			✓	12		12
3	✓	2	13			✓	12		12
4	✓	1	14			✓	11		11
5	✓	2	15	✓	11				11
6	✓	2	16			✓	14		14
7	✓	2						Grand Total	72
8	✓	2							
9	✓	2	91						
10	✓	2							
Total		19	Grand Total					Name and Signature of the Examiner with date	

To be filled by the examiner

Course Outcomes	1	2	3	4	5	6	Total
Marks allotted	17	17	32	34	—	—	100
Marks Obtained	16	15	29	31	—	—	91

IQAC Audit - Remarks

Marks Verified.

S. KANMANI
Name and Signature
of the Member

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Assignment Question Paper

Assignment – 02			Date of Issue:	06.08.2018	Marks	10
Course code	EC6703	Course Title	Embedded and Real Time Systems			
Year	IV	Semester	VII	Date of Submission:	13.08.2018	

Q.No	Questions	CO
1	Software performance optimization.	CO2
2	Applications of Embedded Systems.	CO2

6/8/18

Name and Signature of the Faculty Incharge

G JOHNY

HoD/ECE 6/8/18

S. Gladson.

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DEPARTMENT OF Electronics and Communication Engineering

Assignment Answer Sheet

Name of the Student : M. Padmapriya.

AU Register Number: 732415106028.

Assignment – 02			Date of Issue:	06.08.2018	Marks	10
Course code	EC6703	Course Title	Embedded and Real Time Systems			
Year	IV	Semester	VII	Date of Submission:	13.08.2018	

Q.No	Questions	CO
1	Software performance optimization.	CO2
2	Applications of Embedded Systems.	CO2

Mark Allocation

Rubrics	Marks Allocated	Marks obtained
Content Quality	6	6
Presentation Quality	2	1
Timely submission	2	2
Total marks	10	9

20/8/18

Name and Signature of the Faculty In charge

G. JOHNY

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